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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,492	BEAUCAGE, JEAN	
	Examiner	**Art Unit**	
	Paul Masur	2464	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _27 August 2009_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-39_ is/are pending in the application.

4a) Of the above claim(s) _29_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-28 and 30-39_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _06 July 2006_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. **Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.**

Response to Arguments

2. **Applicant's arguments see page, filed 08/27/2009, with respect to claim 12 have been fully considered and are persuasive.** The objection of claim 12 has been withdrawn.

3. **Applicant's arguments with respect to claims 1-28 and 30-39 have been considered but are moot in view of the new ground(s) of rejection.**

Claim Objections

4. **Claims 1 and 12 are objected to because of the following informalities:** the claim contains optional claim language. The examiner kindly refers the applicant to MPEP § 2106. According to the MPEP, "Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation." The MPEP states that the clause "adapted to" is an example of claim language that suggests a claim limitation is optional.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. **The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:**

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 1-5, 7, 10-15, and 21-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Page (US PG Pub 2005/0213693).

7. **As per claim 1,** Page teaches a system for broadcasting multi-channel signals to a receiving station over a two-wire bus, comprising:

an encoder having:

a multiplexer for multiplexing digital data corresponding to the channel signals and producing a data stream [Page, fig. 5, element 512, paragraph 0080, "During a transmission operation the FPGA 512 performs audio data buffering and framing operations whereas during data reception the FPGA extracts data from the framed structure and converts it back to a DSD stream. The FPGA performs transmission and reception concurrently, implementing a full-duplex audio connection", The FPGA performs both the multiplexing and framing operations.];

a framer connected to the multiplexer, for breaking the data stream up into frames, and for inserting into said frame a header containing at least a predetermined pattern [Page, fig. 5, element 512, paragraph 0080, "During a transmission operation the FPGA 512 performs audio data buffering and framing operations whereas during data reception the FPGA extracts data from the framed structure and converts it back to a DSD stream. The FPGA performs transmission and

reception concurrently, implementing a full-duplex audio connection", The FPGA performs both the multiplexing and framing operations.];

a transceiver with pre-emphasis connected to the framer of the encoder and connectable to the two-wire bus [Page, fig. 5, element 514, paragraph 0080, "The PHY device 514 performs physical layer coding of the framed audio data, implements spectrum control processing and has line drivers that amplify the current and hence the power of the signal to increase its robustness during transmission. The PHY device 514 effectively implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) sub-layers of the physical layer 210", The PHY device performs the emphasis on the output of the encoder before it reaches the two-wire bus.];

a receiver with de-emphasis, connectable to the two-wire bus, said receiver including:

a decoder connectable to the receiving station, the decoder having a de-framer for reproducing the digital data corresponding to selected ones of the multi-channel signals from the frames [Page, fig. 7, paragraph 0083, "The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream", The FPGA, with input from the synchronization clock, determines the unframing operations.], said de-framer being adapted to use a previous frame when an error condition is detected in a current frame [Page, paragraph 0140, "An alternative embodiment uses a modified Frame

Format error detection/correction strategy", A detected error flag causes a frame to be corrected.];

a synchronization circuit using a pattern-oriented phase-locked loop for sampling the incoming data stream using said predetermined pattern, and for regenerating a system clock [Page, fig. 7, paragraph 0084, "The logic signal from the comparator is used to drive a local phase locked loop (PLL) circuit. A phase locked loop (PLL) is an electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. In this case the received high frequency clock signal is the reference signal. The PLL circuit generates a local audio reference clock which is used for reproduction of the DSD audio data", A PLL is used to regenerate the system clock for the DSD audio signal.];

a channel selector circuit connected to the de-framer and controlling which ones of the multi-channel signals are reproduced by the de-framer [Page, fig. 7, paragraph 0083, "The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream", The FPGA, with input from the synchronization clock, determines the unframing operations.]:

at least two data channels, producing multi-channel signals [Page, fig. 6, paragraph 0081, "The clock signal is fed via the RJ45 connector 518 onto a signal pair on the category 5 UTP cable 515 where it is transmitted in parallel with the audio data", Parallel channels imply two data channels with multi-channel signals.];

at least one receiving station [Page, fig. 7, paragraph 0083, “FIG. 7 schematically illustrates reception of the high frequency audio sample clock in parallel with reception of the DSD audio data signal”, The receiving station receives signals from the device in fig. 6.]; and

a single two-wire bus, broadcasting said multi-channel signals from said data channels to each said receiving station [Page, fig. 6, paragraph 0081, “Alternative embodiments may use screened twisted pair cable, which gives enhanced electromagnetic compatibility (EMC) performance”, The twisted pair is a two-wire bus for the multi-channel signals.].

8. **As per claim 2,** Page teaches the system according to claim 1. Page also teaches wherein:

the encoder has delta-sigma analog-to-digital converters for converting the multi-channel signals into digital form for the multiplexer [Page, fig. 5, element 512, paragraph 0080, “During a transmission operation the FPGA 512 performs audio data buffering and framing operations whereas during data reception the FPGA extracts data from the framed structure and converts it back to a DSD stream. The FPGA performs transmission and reception concurrently, implementing a full-duplex audio connection”, The FPGA performs both the multiplexing and framing operations.]; and

the decoder has a delta-sigma digital-to-analog converter connected to the de-framer for converting the digital data corresponding to the selected ones of the multi-channel signals into analog form for the receiving station [Page, fig. 7, paragraph 0083, “The DSD audio signal is received by a transformer 524 and is then supplied to a

physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream", The FPGA, with input from the synchronization clock, determines the unframing operations.].

9. **As per claim 3,** Page teaches the system according to claim 2. Page also teaches wherein the encoder comprises analog interfaces respectively having amplifiers in series with low pass filters for amplifying and filtering the multi-channel signals transmitted to the delta-sigma analog-to-digital converters [Page, fig. 8, elements 552 and 554, paragraph 0085, "As schematically illustrated in FIG. 8, the sample clock processing that occurs in the clock master system involves the low pass filter 552, the differential line driver 554 and the transformer 556", The low pass filter is in series with the line driver, which amplifies the signal.].

10. **As per claim 4,** Page teaches the system according to claim 1. Page also teaches wherein:

the encoder comprises a compression circuit for compressing the digital data input into the framer [Page, fig. 5, element 512, paragraph 0080, "During a transmission operation the FPGA 512 performs audio data buffering and framing operations whereas during data reception the FPGA extracts data from the framed structure and converts it back to a DSD stream. The FPGA performs transmission and reception concurrently, implementing a full-duplex audio connection", The FPGA performs both the multiplexing and framing operations, where data is compressed.]; and

the decoder comprises a decompression circuit for decompressing the digital

data output by the de-framer [Page, fig. 7, paragraph 0083, “The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream”, The FPGA, with input from the synchronization clock, determines the unframing operations, where compressed data is decompressed and reconstituted using the PLLs.].

11. **As per claim 5,** Page teaches the system according to claim 4. Page also teaches wherein the compression circuit and the decompression circuit have look-up tables defining compression and decompression functions respectively [Page, paragraph 0068, “The Physical Coding Sub-layer (PCS) 216 provides a uniform interface to the Reconciliation sub-layer for all 100BASE-TX physical layer entity (PHY) implementations. The PCS 216 provides all services required by the MII including: encoding of MII 4-bit "data nibbles" to 5-bit code groups (and also decoding from 5-bit to data nibbles)”, Tables are used to generate nibbles and form them back into frames.].

12. **As per claim 7,** Page teaches the system according to claim 1. Page also teaches wherein the multiplexer has a time division multiplexing function [Page, fig. 7, DSD signals are time division multiplexed and then reconstructed using the clock signal.].

13. **As per claim 10,** Page teaches the system according to claim 1. Page also teaches wherein the frames comprise a parity bit for data integrity check by the decoder [Page, figs. 23A & 23B].

14. **As per claim 11,** Page teaches the system according to claim 1. Page also teaches wherein the synchronization circuit comprises a sampling circuit for sampling the frames in at a number of times an incoming data rate, a test circuit for testing a phase relation of the frames with an internal reference, and a phase lock loop circuit responsive to the test circuit for phase correction of the synchronization circuit [Page, fig. 7, paragraph 0084, "The logic signal from the comparator is used to drive a local phase locked loop (PLL) circuit. A phase locked loop (PLL) is an electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. In this case the received high frequency clock signal is the reference signal. The PLL circuit generates a local audio reference clock which is used for reproduction of the DSD audio data", A PLL is used to regenerate the system clock for the DSD audio signal.].

15. **As per claim 12,** Page teaches the system according to claim 1. Page also teaches wherein the test circuit is adapted to perform a phase comparison after finding a predetermined bit pattern in the data stream [Page, fig. 7, paragraph 0084, "The logic signal from the comparator is used to drive a local phase locked loop (PLL) circuit. A phase locked loop (PLL) is an electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. In this case the received high frequency clock signal is the reference signal. The PLL circuit generates a local audio reference clock which is used for reproduction of the DSD audio data", A PLL is used to regenerate the system clock for the DSD audio signal.].

16. **As per claim 13,** Page teaches the system according to claim 1. Page also teaches wherein the channel selector circuit comprises a user interface for selection of said ones of the multi-channel signals [Page, paragraph 0057, “with a means of transmitting a serial bit stream between two pieces of equipment”].

17. **As per claim 14,** Page teaches the system according to claim 1. Page also teaches wherein the decoder has a variable gain amplifier for amplifying the selected ones of the multi-channel signals, and a user interface for adjusting a gain of the variable gain amplifier [Page, paragraph 0057, “with a means of transmitting a serial bit stream between two pieces of equipment”].

18. **As per claim 15,** Page teaches the system according to claim 1. Page also teaches wherein the de-framer comprises a synchronization analyzer receiving a signal indicative of the selected ones of the multi-channel signals, and serial to parallel converting circuitry controlled by the analyzer for providing the digital data into parallel form [Page, fig. 7, paragraph 0084, “The logic signal from the comparator is used to drive a local phase locked loop (PLL) circuit. A phase locked loop (PLL) is an electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. In this case the received high frequency clock signal is the reference signal. The PLL circuit generates a local audio reference clock which is used for reproduction of the DSD audio data”, A PLL is used to regenerate the system clock for the DSD audio signal.].

19. **As per claim 21,** Page teaches the system according to claim 1. Page also teaches wherein the multi-channel signals comprise multiple channels of audio stereo

signals, and the receiving station comprises an audio listening station [Page, paragraph 0002, “An example of a problem in data communication will be described in the context of communicating so-called Direct Stream Digital audio data. However, the present invention is applicable to other types of clocked data, such as multi-bit audio data or video data”, High quality audio data is sent to the receiver.].

20. **As per claim 22,** Page teaches the system according to claim 1. Page also teaches wherein the multi-channel signals comprise high speed applications [Page, paragraph 0003, "Direct Stream Digital (DSD) is a high-resolution single-bit audio coding system used for the so-called Super Audio CD consumer disc format"].

21. **As per claim 23,** Page teaches the system according to claim 2. Page also teaches wherein the decoder has at least one additional delta-sigma digital-to-analog converter connected to the de-framer, for converting the digital data corresponding to additional selected ones of the multi-channel signals [Page, fig. 7, paragraph 0083, “The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream”, The FPGA, with input from the synchronization clock, determines the unframing operations.].

22. **As per claim 24,** Page teaches the system according to claim 1. Page also teaches wherein the receiver has outputs for connection to the decoder and to additional like decoders [Page, fig. 7, The receiver is connected to multiple transformers, and therefore, could handle multiple decoders.].

23. **As per claim 25,** Page teaches the system according to claim 1. Page also teaches wherein the two-wire bus forms a serial multi-drop communication network [Page, paragraph 0057, “with a means of transmitting a serial bit stream between two pieces of equipment”].

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Page (US PG Pub 2005/0213693) in view of Wilson et al. (US PG Pub 2006/0122717).

26. **As per claim 6,** Page teaches the system according to claim 4. Page does not teach wherein the compression circuit and the decompression circuit respectively have logarithmic and antilogarithmic functions.

However, Wilson teaches wherein the compression circuit and the decompression circuit respectively have logarithmic and antilogarithmic functions [Wilson, paragraph 0044, " Translation of the linear coefficients fold-down values to logarithmic values that a media codec (and mixer) accepts will be performed in the encoder (or other media content authoring applications)", Encoding and decoding involves logarithmic functions.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Wilson et al. into Page, since Page

suggests a DSD audio transmission system, and Wilson et al. suggests using logarithmic encoding for transmitting streams of digital audio data [Wilson, paragraphs 0002 & 0044] in the analogous art of DSD audio transmissions.

27. Claims 8, 9, 26-28, and 30-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Page (US PG Pub 2005/0213693) in view of Tanaka et al. (US Patent No. 7,236,836).

28. **As per claim 8,** Page teaches the system according to claim 1. Page does not teach wherein said header has less transitions than transitions in the digital data. However, Tanaka et al. teach wherein said header has less transitions than transitions in the digital data [Tanaka, column 5, lines 44-46, "FIG. 18 is a diagram of a structure of 16-bit information containing channel information in a fourth embodiment of this invention", Adding another bit is merely a design choice.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Tanaka et al. into Page, since Page suggests a DSD audio transmission system, and Tanaka et al. suggests the beneficial use of varying frame lengths for DSD audio signals such as to conform to SACD standards [Tanaka, column 30, 14-17] in the analogous art of DCD audio packets.

29. **As per claim 9,** Page teaches the system according to claim 8. Page does not teach wherein the header has a size of 17 bits. However, Tanaka et al. teach wherein the header has a size of 17 bits [Tanaka, column 5, lines 44-46, "FIG. 18 is a diagram of a structure of 16-bit information containing channel information in a fourth embodiment of this invention", Adding another bit is merely a design choice.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Tanaka et al. into Page, since Page suggests a DSD audio transmission system, and Tanaka et al. suggests the beneficial use of varying frame lengths for DSD audio signals such as to conform to SACD standards [Tanaka, column 30, 14-17] in the analogous art of DCD audio packets.

30. **As per claim 26,** Page teaches a method of broadcasting high-speed applications over a serial multi-drop communication network, comprising:

time-division multiplexing the high-speed applications to produce a data stream [Page, fig. 7, DSD signals are time division multiplexed and then reconstructed using the clock signal.]...transmitting the frames with pre-emphasis over the serial multi-drop communication network [Page, fig. 5, element 514, paragraph 0080, "The PHY device 514 performs physical layer coding of the framed audio data, implements spectrum control processing and has line drivers that amplify the current and hence the power of the signal to increase its robustness during transmission. The PHY device 514 effectively implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) sub-layers of the physical layer 210", The PHY device performs the emphasis on the output of the encoder before it reaches the two-wire bus.];

receiving the frames with de-emphasis from the serial multi-drop communication network [Page, fig. 7, paragraph 0083, “The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an

FPGA 528 which unframes the data and produces a DSD bit stream", The FPGA, with input from the synchronization clock, determines the unframing operations.];

detecting a predetermined bit pattern in the received frames [Page, paragraph 0140, "An alternative embodiment uses a modified Frame Format error detection/correction strategy", A detected error flag causes a frame to be corrected.];

synchronizing the received frames using an internal clock signal and an external clock signal found within the frames following a phase comparison made after detection of the predetermined bit pattern [Page, fig. 7, paragraph 0084, "The logic signal from the comparator is used to drive a local phase locked loop (PLL) circuit. A phase locked loop (PLL) is an electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. In this case the received high frequency clock signal is the reference signal. The PLL circuit generates a local audio reference clock which is used for reproduction of the DSD audio data", A PLL is used to regenerate the system clock for the DSD audio signal.];

de-framing the synchronized frames into a selected one of the high-speed applications [Page, fig. 7, paragraph 0083, "The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream", The FPGA, with input from the synchronization clock, determines the unframing operations.]:

producing multi-channel signals with at least two data channels [Page, fig. 6, paragraph 0081, "The clock signal is fed via the RJ45 connector 518 onto a signal pair

on the category 5 UTP cable 515 where it is transmitted in parallel with the audio data", Parallel channels imply two data channels with multi-channel signals.];

utilizing at least one receiving station [Page, fig. 7, paragraph 0083, "FIG. 7 schematically illustrates reception of the high frequency audio sample clock in parallel with reception of the DSD audio data signal", The receiving station receives signals from the device in fig. 6.]; and

broadcasting said multi-channel signals from said data channels to each said receiving station [Page, fig. 7, paragraph 0083, "FIG. 7 schematically illustrates reception of the high frequency audio sample clock in parallel with reception of the DSD audio data signal", The receiving station receives signals from the device in fig. 6.] on a single two-wire bus [Page, fig. 6, paragraph 0081, "Alternative embodiments may use screened twisted pair cable, which gives enhanced electromagnetic compatibility (EMC) performance", The twisted pair is a two-wire bus for the multi-channel signals.].

Page does not teach framing the data stream into frames having a header and a parity bit, the header having a size lower than 32 bits. However, Tanaka et al. teach framing the data stream into frames having a header and a parity bit, the header having a size lower than 32 bit [Tanaka, column 30, lines 17-19, fig. 27, "With reference to FIG. 27, 32-bit audio data have a sequence of a 3-bit head identifier "111", a 1-bit encoding-related flag, 4-bit channel bit information, and 24-bit DSD audio data", The header for the DSD frame is less than 32 bits.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Tanaka et al. into Page, since Page

suggests a DSD audio transmission system, and Tanaka et al. suggests the beneficial use of varying frame lengths for DSD audio signals such as to conform to SACD standards [Tanaka, column 30, 14-17] in the analogous art of DCD audio packets.

31. **As per claim 27,** Page in view of Tanaka et al. teach the method according to claim 26. Page also teaches further comprising analog-to-digital converting the high-speed applications prior to the multiplexing, and digital-to-analog converting the selected one of the high-speed applications after the de-framing [Page, fig. 7, paragraph 0083, “The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream”, The FPGA, with input from the synchronization clock, determines the unframing operations.].

32. **As per claim 28,** Page in view of Tanaka et al. teach the method according to claim 27. Page also teaches wherein the analog-to-digital converting and the digital-to-analog converting comprise over sampling and closed-loop modulating the high-speed applications [Page, fig. 7, paragraph 0083, “The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream”, The FPGA, with input from the synchronization clock, determines the unframing operations.].

33. **As per claim 30,** Page in view of Tanaka et al. teach the method according to claim 26. Page also teaches further comprising parallel to series converting the high-speed applications prior to the multiplexing, and series to parallel converting the selected one of the high-speed applications [Page, fig. 7, paragraph 0083, “The DSD

audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream", The FPGA, with input from the synchronization clock, determines the unframing operations.].

34. **As per claim 31,** Page in view of Tanaka et al. teach the method according to claim 26. Page also teaches further comprising checking data integrity of the synchronized frames using the parity bit [Page, figs. 23A & 23B].

35. **As per claim 32,** Page in view of Tanaka et al. teach the method according to claim 31. Page also teaches wherein a previously received frame is used when an error condition is detected in a currently received frame [Page, paragraph 0140, "An alternative embodiment uses a modified Frame Format error detection/correction strategy", A detected error flag causes a frame to be corrected.].

36. **As per claim 33,** Page in view of Tanaka et al. teach the method according to claim 26. Page also teaches wherein the high-speed applications comprise a multi-channel audio signal broadcast to audio listening stations connected to the serial multi-drop communication network [Page, paragraph 0002, "An example of a problem in data communication will be described in the context of communicating so-called Direct Stream Digital audio data. However, the present invention is applicable to other types of clocked data, such as multi-bit audio data or video data", High quality audio data is sent to the receiver.].

37. **As per claim 34,** Page in view of Tanaka et al. teach the method according to claim 26. Page also teaches wherein the predetermined bit pattern is located in the

header of the frames [Page, paragraph 0140, “An alternative embodiment uses a modified Frame Format error detection/correction strategy”, A detected error flag causes a frame to be corrected.].

38. **As per claim 35,** Page in view of Tanaka et al. teach the method according to claim 26. Page also teaches further comprising compressing the high-speed applications prior to the framing, and decompressing the selected one of the high-speed applications after the de-framing [Page, fig. 7, paragraph 0083, “The DSD audio signal is received by a transformer 524 and is then supplied to a physical layer interface 526 followed by an FPGA 528 which unframes the data and produces a DSD bit stream”, The FPGA, with input from the synchronization clock, determines the unframing operations.].

39. **As per claim 36,** Page in view of Tanaka et al. teach the method according to claim 26. Page also teaches further comprising repeating the frames for transmission over another segment of the serial multi-drop communication Network [Page, paragraph 0057, “with a means of transmitting a serial bit stream between two pieces of equipment”].

40. **As per claim 37,** Page in view of Tanaka et al. teach the method according to claim 26. Page also teaches wherein the repeating comprises sampling the frames in at a number of times an incoming data rate, testing a phase relation with an internal reference, phase correcting the frames going out to the other segment, and transmitting the frames with pre-emphasis to the other segment [Page, fig. 7, paragraph 0084, “The logic signal from the comparator is used to drive a local phase locked loop (PLL) circuit.

A phase locked loop (PLL) is an electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. In this case the received high frequency clock signal is the reference signal. The PLL circuit generates a local audio reference clock which is used for reproduction of the DSD audio data", A PLL is used to regenerate the system clock for the DSD audio signal.].

41. **As per claim 38,** Page in view of Tanaka et al. teach the method according to claim 37. Page also teaches further comprising inserting a clean pulse in the frames, and locking a phase on the clean pulse for sampling the frames [Page, fig. 7, paragraph 0084, "The logic signal from the comparator is used to drive a local phase locked loop (PLL) circuit. A phase locked loop (PLL) is an electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. In this case the received high frequency clock signal is the reference signal. The PLL circuit generates a local audio reference clock which is used for reproduction of the DSD audio data", A PLL is used to regenerate the system clock for the DSD audio signal.].

42. **As per claim 39,** Page in view of Tanaka et al. teach the method according to claim 37. Page also teaches wherein the number of times is higher than a number of times the frames are sampled in the synchronizing [Page, fig. 7, paragraph 0084, "The logic signal from the comparator is used to drive a local phase locked loop (PLL) circuit. A phase locked loop (PLL) is an electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. In this case the received high frequency clock signal is the reference signal. The PLL circuit generates

a local audio reference clock which is used for reproduction of the DSD audio data", A PLL is used to regenerate the system clock for the DSD audio signal.].

43. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Page (US PG Pub 2005/0213693) in view of Watanabe (US PG Pub 2003/0030577).

44. **As per claim 16,** Page teaches the system according to claim 1. Page does not teach further comprising a data repeater connectable between the two-wire bus and an additional two-wire bus, for rebuilding, cleaning up and repeating the frames for transmission on the additional two-wire bus.

However, Watanabe teaches further comprising a data repeater connectable between the two-wire bus and an additional two-wire bus, for rebuilding, cleaning up and repeating the frames for transmission on the additional two-wire bus [Watanabe, fig. 2, element 13, paragraph 0026, "The second output line 21 of the error-detecting and -correcting circuit 12 is connected to an interpolation data generator 13 constituting a feature of this invention. Each time the incoming "error" signal indicates the presence of an error in the recovered delta-sigma modulated audio signal, the interpolation data generator 13 puts out a binary datum for interpolation in place of the detected error", Signals are reconstructed.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Watanabe into Page, since Page suggest a DSD audio stream transmission system, and Watanabe suggests a data

repeater and repairer such as to correct erroneous DSD streams [Watanabe, paragraph 0026] in the analogous art of DSD streams.

45. **As per claim 17,** Page in view of Watanabe teaches the system according to claim 16. Page teaches the system further comprising a transceiver with pre-emphasis connected to the data repeater and connectable to the additional two-wire bus [Page, fig. 5, element 514, paragraph 0080, "The PHY device 514 performs physical layer coding of the framed audio data, implements spectrum control processing and has line drivers that amplify the current and hence the power of the signal to increase its robustness during transmission. The PHY device 514 effectively implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) sub-layers of the physical layer 210", The PHY device performs the emphasis on the output of the encoder before it reaches the two-wire bus.].

Page does not teach wherein: the data repeater comprises a sampler for sampling the frames in at a number of times an incoming data rate, a test circuit for testing a phase relation with an internal reference, a feedback circuit responsive to the test circuit for correction of the internal reference used by the sampler and the test circuit, and a correction circuit for phase correction of the frames going out from the repeater.

However, Watanabe teaches wherein: the data repeater comprises a sampler for sampling the frames in at a number of times an incoming data rate, a test circuit for testing a phase relation with an internal reference, a feedback circuit responsive to the

test circuit for correction of the internal reference used by the sampler and the test circuit, and a correction circuit for phase correction of the frames going out from the repeater [Watanabe, fig. 2, element 13, paragraph 0026, “The second output line 21 of the error-detecting and -correcting circuit 12 is connected to an interpolation data generator 13 constituting a feature of this invention. Each time the incoming "error" signal indicates the presence of an error in the recovered delta-sigma modulated audio signal, the interpolation data generator 13 puts out a binary datum for interpolation in place of the detected error”, Signals are reconstructed.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Watanabe into Page, since Page suggest a DSD audio stream transmission system, and Watanabe suggests a data repeater and repairer such as to correct erroneous DSD streams [Watanabe, paragraph 0026] in the analogous art of DSD streams.

46. **As per claim 18,** Page in view of Watanabe teaches the system according to claim 17. Page does not teach wherein the data repeater has a phase locked on one clean pulse intentionally generated by the encoder, the frames being sampled by the sampler based on the phase.

However, Watanabe teaches wherein the data repeater has a phase locked on one clean pulse intentionally generated by the encoder, the frames being sampled by the sampler based on the phase [Watanabe, fig. 2, element 13, paragraph 0026, “The second output line 21 of the error-detecting and -correcting circuit 12 is connected to an interpolation data generator 13 constituting a feature of this invention. Each time the

incoming "error" signal indicates the presence of an error in the recovered delta-sigma modulated audio signal, the interpolation data generator 13 puts out a binary datum for interpolation in place of the detected error", Signals are reconstructed.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Watanabe into Page, since Page suggest a DSD audio stream transmission system, and Watanabe suggests a data repeater and repairer such as to correct erroneous DSD streams [Watanabe, paragraph 0026] in the analogous art of DSD streams.

47. **As per claim 19,** Page in view of Watanabe teaches the system according to claim 17. Page does not teach wherein the correction circuit comprises a digital filter.

However, Watanabe teaches wherein the correction circuit comprises a digital filter [Watanabe, fig. 2, element 15, paragraph 0035, "The interpolation data switch 24 is connected between interpolation data generator 13 and DAC 15 for on-off operation in inverse relationship to the primary data switch 23", The DAC handles the filtering functionality.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Watanabe into Page, since Page suggest a DSD audio stream transmission system, and Watanabe suggests a data repeater and repairer such as to correct erroneous DSD streams [Watanabe, paragraph 0026] in the analogous art of DSD streams.

48. **As per claim 20,** Page in view of Watanabe teaches the system according to claim 17. Page does not teach wherein the number of times is higher than a number of times the frames are sampled by the decoder.

However, Watanabe teaches wherein the number of times is higher than a number of times the frames are sampled by the decoder [Watanabe, fig. 2, element 13, paragraph 0026, “The second output line 21 of the error-detecting and -correcting circuit 12 is connected to an interpolation data generator 13 constituting a feature of this invention. Each time the incoming "error" signal indicates the presence of an error in the recovered delta-sigma modulated audio signal, the interpolation data generator 13 puts out a binary datum for interpolation in place of the detected error”, Signals are reconstructed.].

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the teachings of Watanabe into Page, since Page suggest a DSD audio stream transmission system, and Watanabe suggests a data repeater and repairer such as to correct erroneous DSD streams [Watanabe, paragraph 0026] in the analogous art of DSD streams.

Conclusion

49. **Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.** Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

50. **The Examiner has cited particular columns and line numbers or paragraphs in the references applied to the claims above for the convenience of the applicant.** Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, the Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

51. **If the Applicant is of the opinion that an interview would help advance prosecution in this case, they are welcome to call the Examiner, Paul Masur, at**

the number listed below to schedule an interview. The Examiner prefers interview requests be accompanied with a detailed agenda via fax. The Examiner's fax number is (571) 270-8297. The Examiner is willing to consider proposed amendments, clarify rejections, and discuss any other issues that are presented by the Applicant. Please note that the Examiner may not be able to accommodate all requests due to scheduling constraints. It is recommended that interview requests be sent with ample time to schedule an interview.

52. **Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Masur whose telephone number is (571) 270-7297.** The examiner can normally be reached on Monday through Friday from 7:00AM to 4:30PM (Eastern Time).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2464

/P. M./
Examiner, Art Unit 2464